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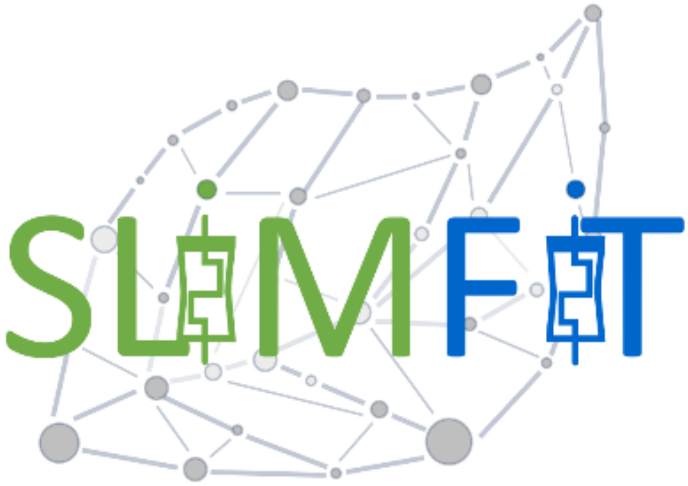
SLIMFIT

SMART LOGIC-IN-MEMORY FOR THE INTERNET OF THINGS



D3.1 EXPERIMENTAL ASSESSMENT OF SIMPLY PARADIGM

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EXECUTIVE SUMMARY

In this deliverable we report about the design, development, realization, and testing of an evaluation platform based on an FPGA and a custom PCB. The platform is designed to be able to control an array of memristors to execute the core operations of the SIMPLY logic scheme. Upon successful verification of the platform functionality, the packaged memristive devices from Knowm were characterized using the platform, and then the feasibility of the SIMPLY core operations was verified. For all of the 1-bit and 2-bit core operations, the energy consumption was measured and then compared with the results from the simulations of the integrated design of the full SIMPLY cell, reported earlier in D2.1, and with preliminary measurements from a test chip on which the building blocks of the full SIMPLY cell were realized. The energy estimates were performed at different speeds (i.e., different pulse widths for the core operations) in order to verify the scaling trends of the energy consumption with the operation speed. The measured results and the comparison of their linear projections to the speed typical of IC designs with the results from D2.1 and those attained on the test chip confirm the energy efficiency advantage of the SIMPLY architecture compared to traditional digital systems. Finally, we envision interesting additions and future developments, which constitute the ground for activities beyond the horizon of the SLIMFIT project with the aim of capitalizing on the obtained results.

CONTENTS

1 CIRCUIT ARCHITECTURE

1.1 GENERAL STRUCTURE

In this Section we discuss the general structure of the evaluation platform able to control an array of memristors to realize the core operations of the SIMPLY logic scheme. The aim is to measure the energy consumption associated with these logic operations within the possibility of the FPGA specifications in terms of pulse width. Results are then projected to the nanosecond regime to estimate the attainable performance of this ultra-low power approach when run at GHz speed in fully-integrated Very Large Scale of Integration (VLSI) chips. The comparison with the simulations in D2.1 and with preliminary measurements on a dedicated test chip (fabricated within the context of a different research project) provides insights into the role played by the memristive technology and the CMOS peripheral circuitry on the overall energy efficiency and performance. The entire system is composed by a DE1-SoC 5CSEMA31C6F (Cyclon V) FPGA, a custom digital-to-analog interface (DAI) realized on a PCB, and an array of 8 Knowm memristors with a pull-down resistor, see Fig. 1-1.

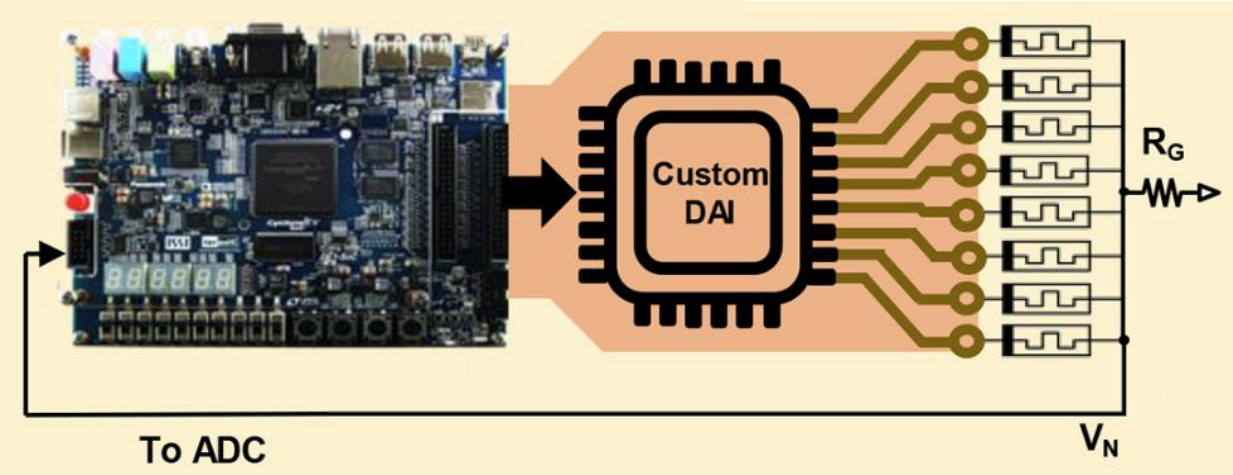

FIGURE 1-1: SCHEMATIC OF THE FPGA-BASED PLATFORM, COMPOSED BY THE FPGA, THE DEVELOPED CUSTOM DAI AND THE ARRAY OF PACKAGED SDC KNOWM MEMRISTORS WITH A PULL-DOWN RESISTOR R_G. V_N IS READ BY THE FPGA ADC, WHILE THE CUSTOM DAI IS FED BY THE GPIO PINS OF THE FPGA.

The platform is designed to handle n ($1 \leq n \leq 8$) memristors and to provide different pulse widths and amplitudes for the required signals to be applied to the top electrode of the memristors (V_{READ}, V_{SET}, V_{RESET}). Three different operation modes can be outlined: *i*) operations on a single specific device, fundamental for S-FALSE and SET operations, requiring the system to ensure also negative pulses; *ii*) operations on two devices, as SIMPLY requires the application of simultaneous driving voltages on two different devices to perform the 2-bit READ operation; *iii*) operations on n devices, since complex logic operations can benefit from the execution of the n-SIMPLY operation with more than two inputs [1]. A simultaneous read pulse on more than two memristors must be applied in this case. Although here we do not explore this possibility, the platform is conceived to allow this operation mode for future studies. All these modalities can be performed 'manually' or in a pre-defined sequence guided by the specific FPGA code. The employed FPGA provides, in fact, ten switches and four buttons that can be each linked to a specific function. Eight switches are used as memristors selectors, initializing the needed enabling signals to drive the correct devices. The buttons array activates the fundamental functions. Three of them are dedicated to start the READ, SET, and RESET operations on the memristors selected by the switches. In this way, each device can be read, driven in HRS or LRS independently. The platform is also conceived to support the execution of the operations typical of the conventional IMPLY approach, though this option is not actively explored here. However, for this purposes, another switch ($V_{COND-ENABLE}$) allows to enable the presence of a positive pulse, different from V_{SET}, during IMPLY – since the latter makes use of a pair of voltages, V_{SET} and V_{COND}, applied simultaneously to two different devices. The portion of the DAI devoted to the generation of the V_{COND} voltage is highlighted in yellow in Fig. 1-2. The pulse widths are programmed by means of a Pulse Width Modulation (PWM) VHDL component. The FPGA General Purpose Input/Output (GPIO), composed by 40 pins, supports only digital signals, consisting in a logic-0 of 0 V and a logic-1 of 3.3 V. The programmed PWM in the FPGA logic can only handle the output signal pulse width and not its amplitude, stressing the necessity for a proper conditioning circuit. Therefore, we implemented a custom DAI that allows to transfer the correct input voltages to the respective memristors, see Fig. 1-1 and Fig. 1-2. It is composed by: *i*) 2 digital potentiometers (MCP41010), ranging from 0 to 10 kΩ

with 256 programmable taps; *ii*) 3 analog tri-state buffers (TS12A12511); *iii*) 8 4-channel analog multiplexers (TMUX6104); *iv*) 2 operational amplifiers; *v*) 1 2-inputs OR; *vi*) 1 n-MOSFET (ZVN2106A); *vii*) 7 resistors. The general schematic of the platform is reported in Fig. 1-2.

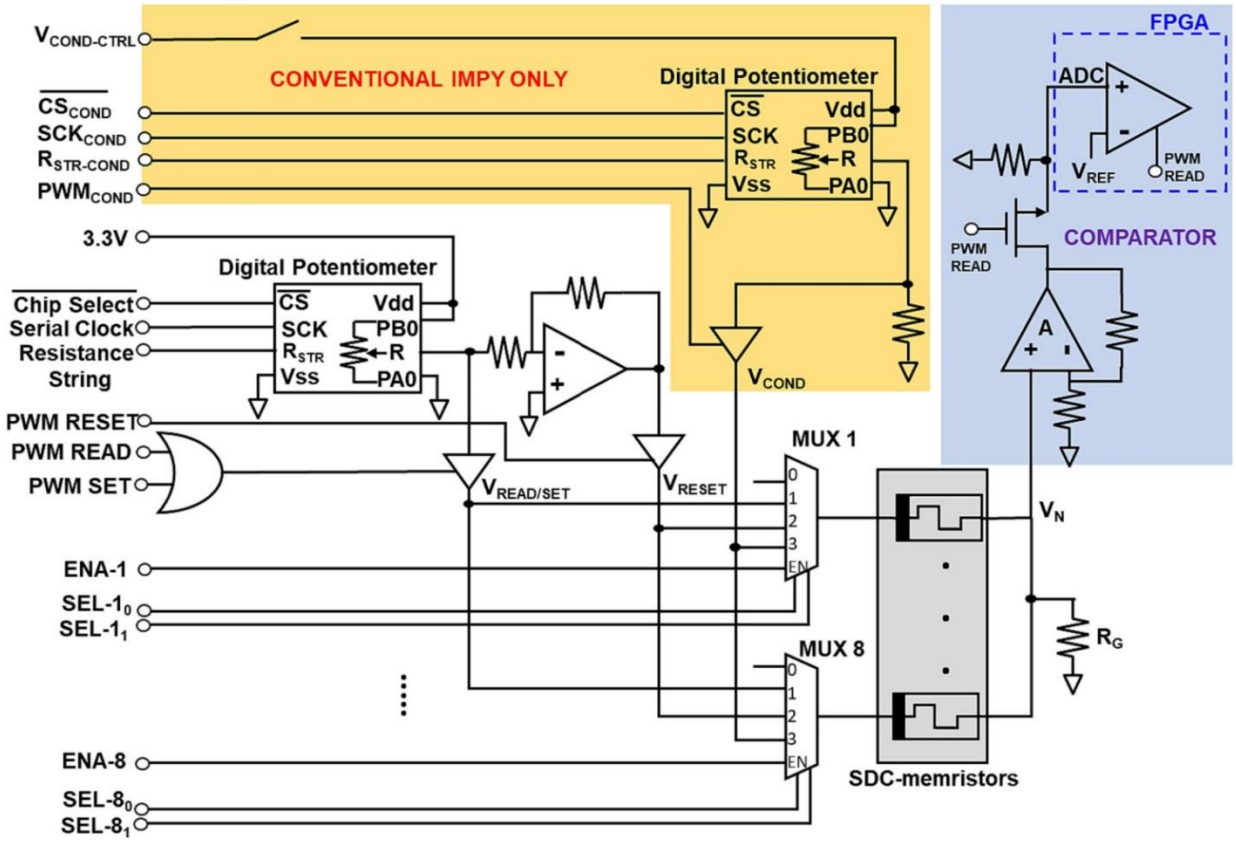

FIGURE 1-2: SCHEMATIC OF THE CUSTOM DAI CONNECTED TO THE MEMRISTORS ARRAY AND TO THE ADC INTERNAL TO THE FPGA. IN YELLOW, THE CIRCUIT DEDICATED TO IMPLEMENTING V_{COND} (ONLY FOR CONVENTIONAL IMPLY). IN BLUE, THE COMPARATOR CIRCUIT.

The memristors are selected by means of an array of multiplexers. Each multiplexer is connected to the top electrode of a single memristor and is activated through a digital enable pin (ENA-1, ENA-2, …, ENA-8, see Fig. 1-2). When enabled, the output of the multiplexer is driven depending on the desired operation (READ, SET, or RESET), which is determined by the state of the selector bits ($sel\text{-}1_0$, $sel\text{-}1_1$, $sel\text{-}2_0$, $sel\text{-}2_1$, …, $sel\text{-}8_0$, $sel\text{-}8_1$, see Fig. 1-2). When a memristor is not selected, its top electrode is kept floating by the tri-state I/O pins of the FPGA. The output voltages are adjusted using programmable digital potentiometers in a voltage divider configuration. One digital potentiometer is used to generate both V_{SET} and V_{READ}, while the other is used to generate V_{COND} for the IMPLY option (yellow area in Fig. 2-1). V_{RESET} is also determined by the gain of the associated operational amplifier in inverting configuration, which receives V_{SET} as an input. For each READ, SET, RESET operation, the respective enabling PWM signal activates an analog tri-state buffer only for a determined period of time, which allows the signal transmission to the multiplexer array, sending the pulse only to the selected memristors. An amplifier is used to boost the V_N signal before the comparator, that is implemented directly inside the FPGA by means of the ADC, thus improving the signal to noise ratio (blue area in Fig. 1-2). The comparison, obviously, is done only during the READ operation. To avoid the possibility of the ADC input experiencing negative transient voltage during the RESET operation, a n-MOSFET and a resistor are placed before the ADC pin to realize a pull-down action.

1.2 FIELD-PROGRAMMABLE GATE ARRAY

The FPGA adoption provides the possibility to instantiate the desired hardware, programmed using VHDL and Verilog languages, with a clever exploitation of the system resources. In particular, for this application the FPGA platform employs only 2% of logic utilization (601/32070), expressed in Adaptive Logic Module (ALM); the number of used registers is 703, the number of pins is 87/457 (19%), and the number of employed DSP blocks (containing shift registers) is 4/87 (5%). The DE1-SoC 5CSEMA31C6F (Cyclon V) FPGA implements an internal clock signal at 50 MHz, enabling the creation of multiple timing signals for each virtual block. The internal ADC features 8 channels with a 12-bits resolution, and input voltage allowed in the range

of 0–4.096 V, with a sample read frequency up to 40 MHz. Only one channel is needed in our case, which receives the feedback signal V_N to be then compared with a specifically sized V_{TH}.

1.3 Custom Printed Circuit Board

The DAI in Fig. 1-2 was realized on a custom PCB using EasyEDA. The connection to the FPGA outputs (that constitute inputs to the interface on the PCB) is implemented via a 2x20 IDC male socket with 2.54 mm pitch. As shown in Fig. 1-3, a dual supply (± 5 V) is included to fully support the operational amplifiers, specifically the one devoted to the generation of the V_{COND} signal, though not used in this assessment. In addition, a dedicated 3.3 V supply line is included to provide the voltage to the digital potentiometer devoted to the generation of the V_{SET} and V_{READ} voltages, as also reported in Fig. 1-2. The top and bottom layers of the PCB design are reported in Fig. 1-3 and Fig. 1-4, respectively.

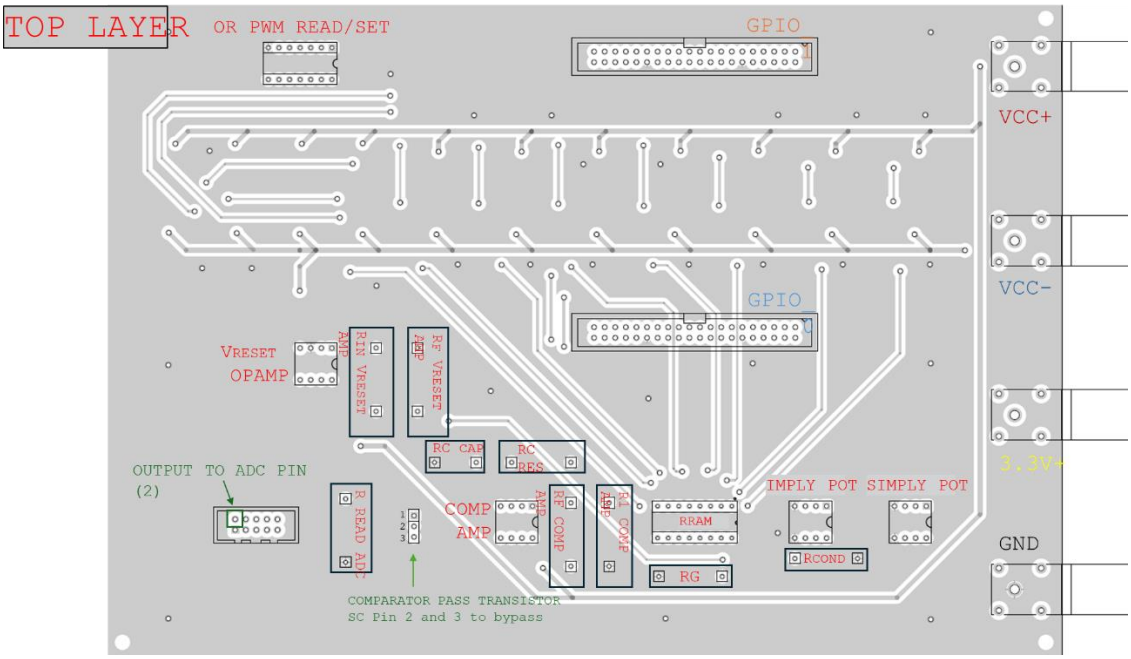

Figure 1-3: Top layer of the PCB design.

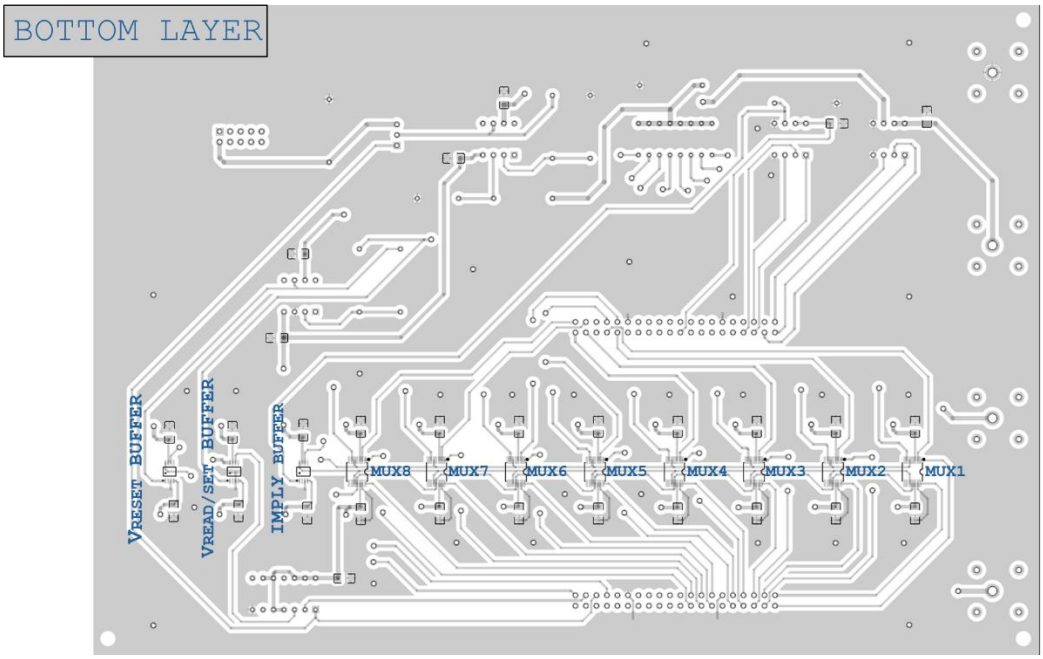

Figure 1-4: Bottom layer of the PCB design.

After design validation, the PCB was fabricated and tested to check the correctness of all electrical links. Then, all the components were first individually tested to check their functionality and then soldered on the PCB or mounted on the corresponding sockets. After assembly, the PCB was connected to the power supply lines and to the FPGA to allow a general testing of the platform, which was successfully completed. A photograph of the fabricated custom PCB (top layer facing up) taken during the testing phase is shown in Fig. 1-5, where the connectors to the FPGA outputs and inputs are clearly visible (rainbow and grey flat cables, respectively). The coloured banana connectors to the power supply lines are on the left, while the oscilloscope probes used to monitor key signals are on the top side.

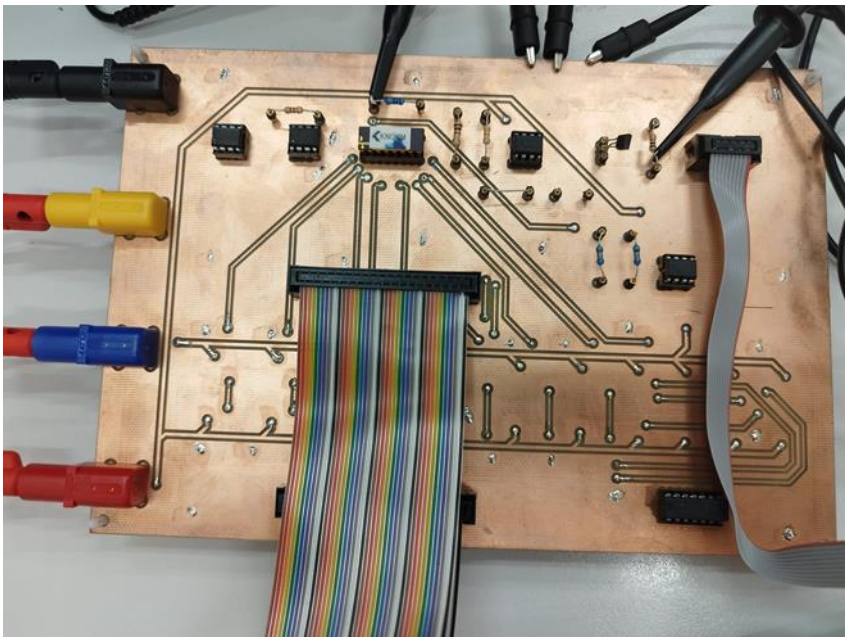

FIGURE 1-5: PHOTOGRAPH OF THE FABRICATED CUSTOM PCB. THE CONNECTORS TO THE FPGA OUTPUTS (RAINBOW FLAT CABLE) AND TO THE FPGA INPUTS (I.E., TOWARD THE ADC, GREY FLAT CABLE) ARE VISIBLE, AS WELL AS THE LINKS TO THE POWER SUPPLY LINES (COLOURED BANANA CONNECTORS ON THE LEFT) AND THE OSCILLOSCOPE PROBES (TOP).

2 PACKAGED MEMRISTOR CHARACTERIZATION

The memristors employed in this experimental assessment, called Self-Directed Channel (SDC), are developed by Knowm Inc. [2] and are available in a 16-pin Dual In-line Package (16-DIP) configuration, as sketched in Fig. 2-1. In this section, we report the details of their characterization aimed at verifying their potential in the proposed logic-in-memory scheme. Differently from metal-oxide RRAMs [3], which rely on the formation and dissolution of a conductive filament for the switching mechanism, these SDC memristors are ion-conducting devices that change their resistance due to the movement of Ag^+ ions into the device structure [4].

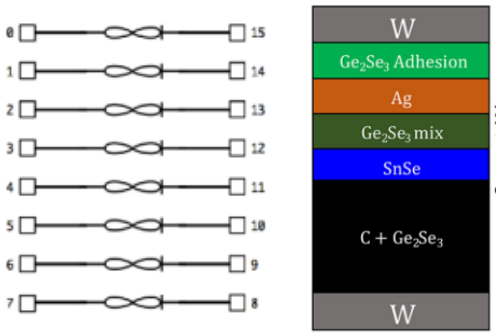

FIGURE 2-1: (LEFT) PINOUT OF THE 16-DIP SHOWING THE 8 AVAILABLE SDC DEVICES. (RIGHT) SCHEMATIC REPRESENTATION OF THE STACK OF AN SDC MEMRISTOR.

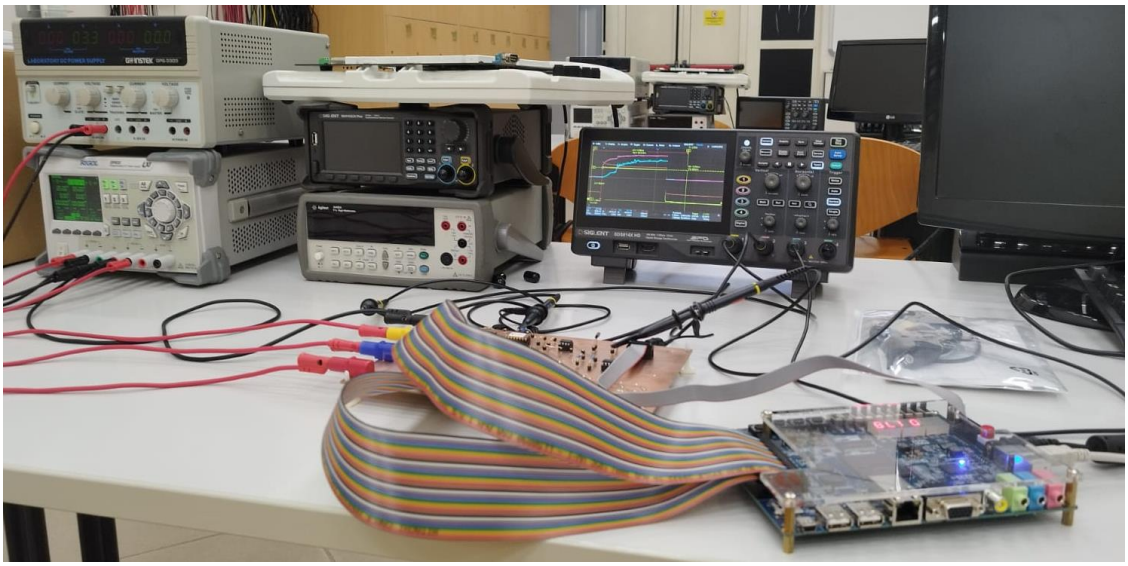

FIGURE 2-2: PHOTOGRAPH OF THE EMPLOYED MEASUREMENT SETUP, THAT INCLUDES A SIGLENT SDG1022X PLUS FUNCTION GENERATOR, A SIGLENT SDS814X HD OSCILLOSCOPE, A GWINSTEK GPS-3303 REGULATED LABORATORY DC POWER SUPPLY (+ 3.3V), A RIGOL DP832 REGULATED LABORATORY DC POWER SUPPLY (± 5V), THE CUSTOM PCB AND THE DE1-SOC 5CSEMA31C6F (CYCLON V) FPGA.

Fig. 2-1 shows the stack layout of the devices. Despite the high number of thin layers, the fabrication mechanism is simple and reliable. In fact, the deposition of all layers, including the top electrode, is done in-situ in one processing step by means of sputtering. The constant separation between the Ag-source, consisting in the Ge_2Se_3/Ag/ Ge_2Se_3 layers, and the top electrode, allows also high temperature processes and operations, including long-term continuous operation at 150 °C [4]. Also, no high voltage forming step is required, meaning that the same set voltage required during the normal device operation can be used to switch a pristine device into a low resistance state [5]. Furthermore, the required programming voltages and compliance current values are lower with respect to classical metal-oxide RRAMs [3], with a consequent decrease in power consumption. Each package is constituted by eight discrete SDC devices that are initially in a high resistance state (MΩ – GΩ range) [6]. The first set operation generates Sn ions from the SnSe layer and forces them into the active Ge_2Se_3 layer. Sn ions, in fact, are expected to facilitate the incorporation of Ag into the active layer at the Ge-Ge bonding sites [6]. This occurs through an energetically favourable process in which the electrons entering the active layer from the negative bottom electrode, concurrently with the formation of Sn ions from the SnSe layer, enable formation of a pair of self-trapped electrons in the Ge_2Se_3 active layer strongly localized around the Ge-Ge dimers present in this Ge-rich glass [6]. This results in the distortion of the Ge-Ge bond by means

of the reaction with Ag, creating an 'opening' near the Ge-Ge sites, providing the access for Ag^+ and creating a natural conductive self-directed channel within the active layer for the movement of Ag^+ during device operation, since Ag has a tendency to agglomerate with other Ag atoms. This pathway does not consist in a conductive metallic filament between the two electrodes, but it is simply a channel with a resistance imposed by the varying concentrations of Ag within it. The resistance is tuneable in the lower and higher directions by movement of Ag onto or away from these agglomeration sites through application of either a positive (set) or negative (reset) potential, respectively, across the device [5].

These devices have been characterized using the measurement setup in Fig. 2-2, which includes a SIGLENT SDG1022X Plus function generator, a SIGLENT SDS814X HD oscilloscope, a GWINSTEK GPS-3303 regulated laboratory DC power supply (+ 3.3V), a Rigol DP832 regulated laboratory DC power supply (± 5V), as well as the custom PCB and the DE1-SoC 5CSEMA31C6F (Cyclon V) FPGA discussed in Section 1.

2.1 QUASI-STATIC CHARACTERISTICS

For the quasi-static characterization of the individual SDC devices, the function generator is used to apply different voltage stimuli to the series of one SDC memristor and one 10 kΩ resistor (R_G) with 5% tolerance. The resistor and the SDC memristor are placed on the custom prototyping PCB on which appropriate sockets to accommodate the 16-DIP memristor chip and the resistor are soldered. The voltage stimuli are applied to the series connection of the two devices, while the current flow is computed from the voltage drop across the resistor R_G, the latter measured via the oscilloscope. The goal is to verify which memristor SDC device among the 8 available in a single package is functional.

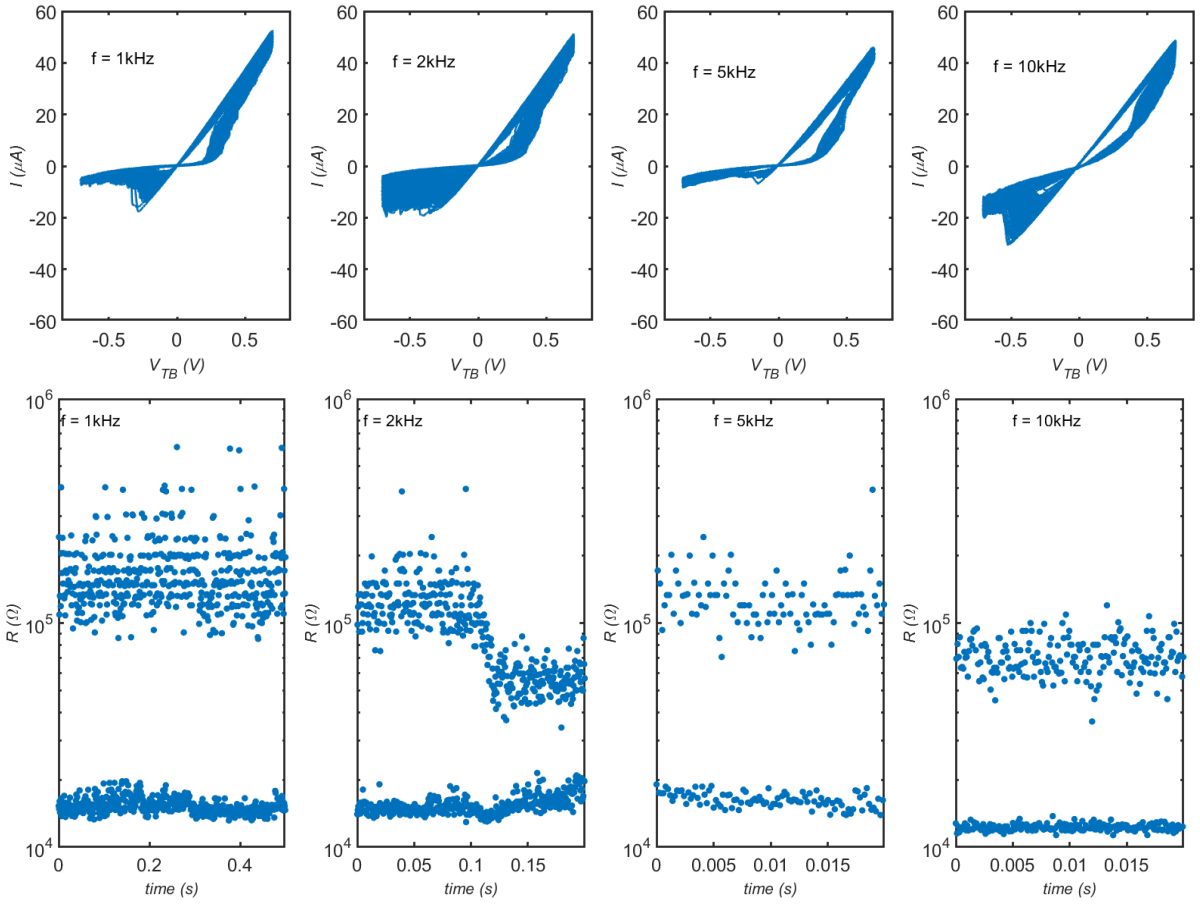

FIGURE 2-3: (TOP) I-V CHARACTERISTIC CURVES OF AN SDC MEMRISTOR UNDER SINUSOIDAL VOLTAGE STIMULI WITH A PEAK-TO-PEAK AMPLITUDE V_{PP} = 1.4V AT DIFFERENT FREQUENCIES, RANGING FROM 1 KHZ TO 10 KHZ (LEFT TO RIGHT). (BOTTOM) CORRESPONDING RESISTANCE VALUE EXTRACTED FROM THE I-V CURVES AT A READ VOLTAGE V_{READ} = 50 MV, WHICH INCLUDES THE CONTRIBUTION OF THE 10 KΩ SERIES RESISTOR.

Fig. 2-3 reports, in the top panels, the measured I-V characteristic under sinusoidal voltage stimuli with a peak-to-peak amplitude V_{PP} = 1.4V at different frequencies, ranging from 1 kHz to 10 kHz. For each case, at least 100 switching cycles are performed. The bottom panels show the resistance value extracted from the I-V curves at a read voltage V_{READ} = 50 mV, which includes the contribution of the 10 kΩ series resistor. For these plots, the *x*-axis reports the time at which each resistance value was measured during the application of the sinusoidal

stimulus to the series of the SDC device and the 10 kΩ resistor (so that the different points on the plot all have an *x*-coordinate value that is the time at which the input waveform value was equal to V_{READ}). The results clearly show that a satisfactory and repeatable memory window, nearly one order of magnitude wide, can be obtained in all conditions. Notice that the compliance current that is enforced by the 10 kΩ resistor is around 50 μA, which has been reported to be high enough to stabilize the created channel and minimize the short-term plasticity effect (i.e., short-term resistance drift) [2, 4-6]. Similar results, shown in Fig. 2-4, are obtained when applying a triangular voltage stimulus with the same V_{PP} and at frequencies in the same range. However, in this case the obtained memory window is somewhat smaller, which is expected since the memristors experience a less intense cumulative voltage stress due to the different waveform shape.

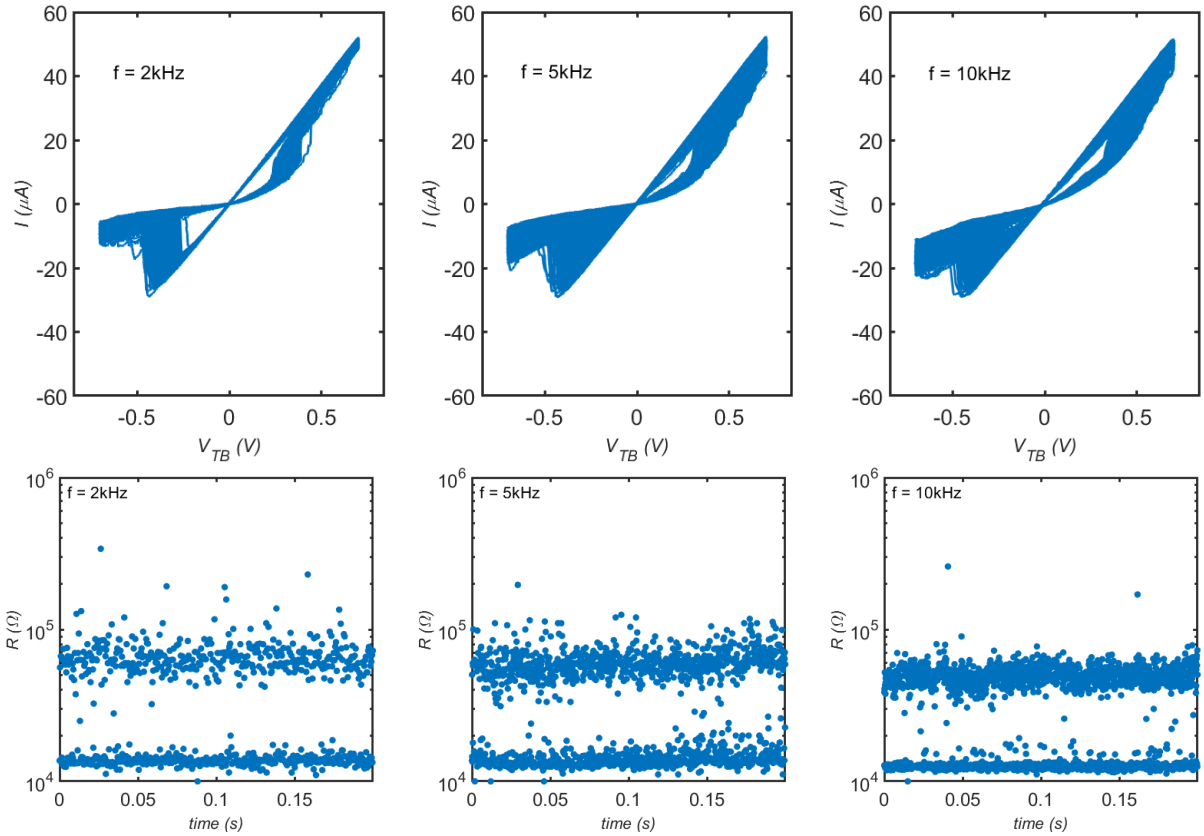

FIGURE 2-4: (TOP) I-V CHARACTERISTIC CURVES OF AN SDC MEMRISTOR UNDER TRIANGULAR VOLTAGE STIMULI WITH A PEAK-TO-PEAK AMPLITUDE V_{PP} = 1.4V AT DIFFERENT FREQUENCIES, RANGING FROM 1 KHZ TO 10 KHZ (LEFT TO RIGHT). (BOTTOM) CORRESPONDING RESISTANCE VALUE EXTRACTED FROM THE I-V CURVES AT A READ VOLTAGE V_{READ} = 50 MV, WHICH INCLUDES THE CONTRIBUTION OF THE 10 KΩ SERIES RESISTOR.

2.2 HIGH-RESISTANCE STATE RETENTION

One of the main characteristics of the SIMPLY platform is the ability to avoid unnecessary stress to the memristors by virtue of the preliminary READ step, which dramatically reduces the read disturb effect and extends the state retention of the device.

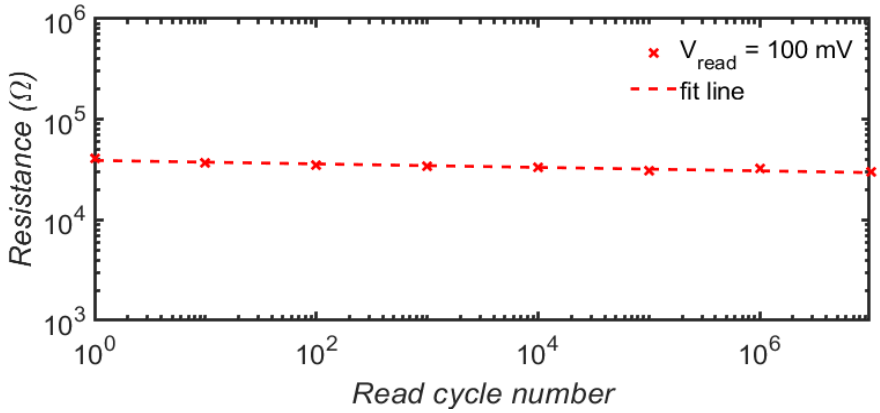

FIGURE 2-5: READ- INDUCED DEGRADATION OF HRS RESISTANCE UNDER PULSED (10^{-5} S) READ AT V_{READ} = 100 MV.

Since only positive voltages are used to perform the READ operation, the only resistive state that is required to withstand the READ operation without showing significant resistance degradation is the high-resistance state (HRS). Therefore, it is mandatory to check whether the SDC devices under test are able to show a sufficient state retention in HRS when subject to an extended sequence of READ pulses. Notably, the in-operation logic retention for the devices employed in the FPGA-based platform was one of the target key performance indicators (KPIs) identified in the project proposal – with a target of 10^6 instructions (i.e., tolerance to a train of at least 10^6 READ pulses). Using the pulse waveform of the function generator, the memristors devices are then first set and subsequently reset using 10^{-5} s pulses with ±1.5V amplitude. Then, to assess the HRS read induced degradation, bursts of 10^{-5} s pulses with V_{READ} = 100 mV amplitude were applied to the device and the resistance measured with the same voltage pulses at decade intervals, up to 10^7. The time duration of the read pulse was chosen to be 10^{-5} s since it is the shortest pulse that can be achieved with the FPGA-based platform. The value of V_{READ} was intentionally chosen to be higher than that adopted for the device quasi-static characterization in order to provide a higher read disturb stress to the device. The results, reported in Fig. 2-5, show negligible HRS resistance degradation across 10^7 cycles, even with V_{READ} = 100 mV.

3 CHARACTERIZATION OF SIMPLY CORE OPERATIONS

In this Section we report about the characterization of the SIMPLY core operations (i.e, RESET, SET, 1-bit READ, 2-bit READ) required by the SIMPLY architecture. Each core operation was tested using the manual operation feature of the PCB which allows to select on which of the 8 memristors available in each chip to perform the main core operations. Different voltages and pulse widths were tested by appropriately reprogramming the FPGA between tests. To estimate the energy per operation, the voltage at the top electrode (V_{TE}) and the voltage across the 10 kΩ pull-down resistor (V_N) were recorded with the oscilloscope.

3.1 1-BIT CORE OPERATIONS

In Fig. 3-1, we report the results of the characterization of the 1-bit core operation. Specifically, in the case of the results in Fig. 3-1, both SET, RESET, and READ pulses are 1 ms long. However, the results were also verified for different pulse durations. The voltage amplitude used for the SET operation, V_{SET}, is measured to be 2.7 V which is close to the target programmed value of 3 V (for which the digital potentiometer was set). The voltage amplitude used for the RESET operation, V_{RESET}, is measured to be -1.98 V, close to the target programmed value of -2 V (for which the digital potentiometer was set). After SET and RESET, the device resistance was measured by means of the 1-bit READ operation, using V_{READ} = 100 mV. It is clear from Fig. 3-1 that the both the SET and the RESET operations are much faster than the applied 1 ms pulse width. This is especially visible in the RESET trace, which shows how the current in the SDC device (proportional to the voltage across the pull-down resistor, V_N) strongly and quickly decreases upon the application of the RESET pulse to the top electrode of the SDC device. In agreement with the results of the quasi-static characterization, the values of V_N measured by means of the 1-bit READ operation after SET and RESET, respectively, are quite different. This not only implies that the SET and RESET pulses correctly change the device resistance, but also that the correct readout of the SDC resistive state can be performed via the 1-bit READ operation (i.e., a clear difference exists between the two V_N values recorded after SET and RESET).

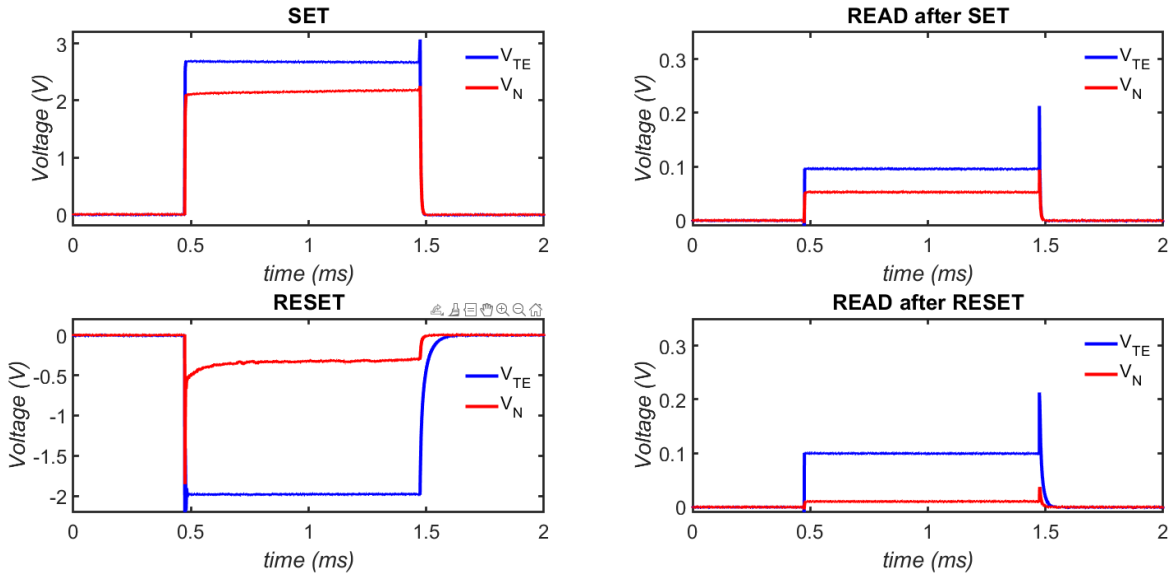

FIGURE 3-1: VERIFICATION OF THE 1-BIT CORE OPERATIONS USING PULSE WIDTH = 1 MS FOR ALL OPERATIONS. THE MEASURED VALUE OF V_{SET} = 2.7 V (3 V TARGET PROGRAMMED WITH THE DIGITAL POTENTIOMETER). THE MEASURED VALUE OF V_{RESET} = = -1.98 V (-2 V TARGET PROGRAMMED WITH THE DIGITAL POTENTIOMETER). V_{READ} = 100 MV.

3.2 2-BIT READ OPERATION

Like in Section 3.1, we here report the results of the characterization of the 2-bit READ operation. Specifically, the results in Fig. 3-2 show the outcomes in the four possible combinations of the two input bits (i.e., the two SDC devices involved in the computation). Naturally, before each 2-bit READ operation, the devices were opportunely set to the target resistive state (either HRS for logic 0 or LRS for logic 1) by means of individual SET or RESET operations. The details of the SET and RESET pulses are the same as those reported in Section 3.1. In this case, the 2-bit READ operation is performed by applying simultaneously a READ pulse to the top electrodes of both involved SDC devices. For the results in Fig. 3-2, READ pulses are 1 ms long. However, the results were also verified for different pulse durations. The voltage amplitude used for the SET, RESET,

and 2-bit READ operations are identical to those reported in Section 3.1 for the 1-bit core operations. After SET and RESET, the device resistance was measured by means of the 1-bit READ operation, using V_{READ} = 100 mV. It is clear from Fig. 3-2 that the voltage across the pull-down resistor, V_N, is significantly lower in the 00 case (i.e., when both devices are in HRS) than in all the other cases (i.e., when at least one of the devices is in LRS). This implies that a good read margin exists and that the 2-SIMPLY operation can be reliably performed with the proposed platform.

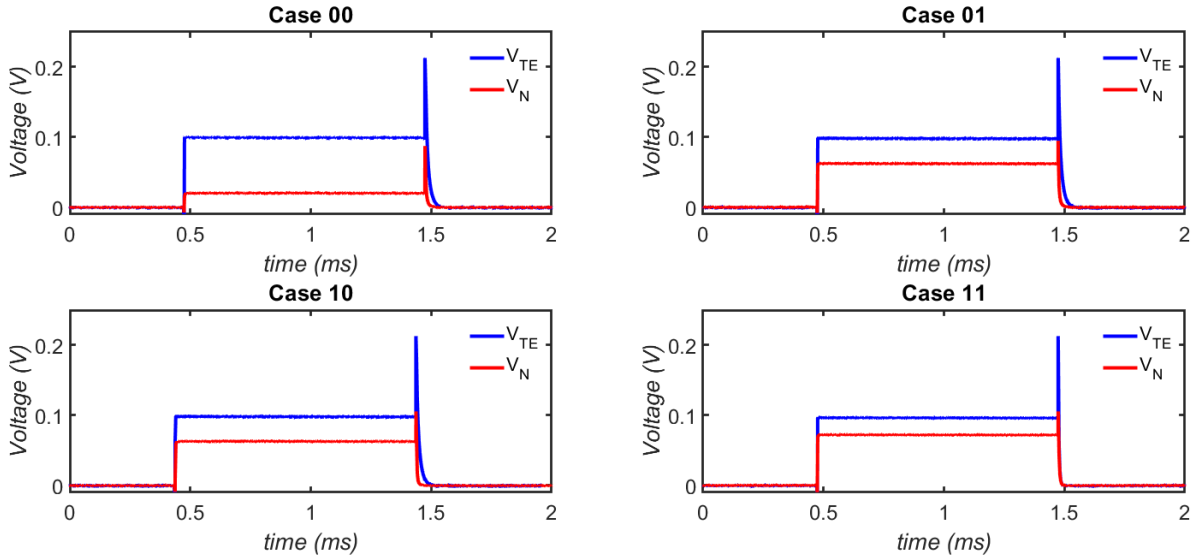

FIGURE 3-2: VERIFICATION OF THE 2-BIT READ OPERATION USING PULSE WIDTH = 1 MS FOR ALL OPERATIONS. THE MEASURED VALUE OF V_{SET} = 2.7 V (3 V TARGET PROGRAMMED WITH THE DIGITAL POTENTIOMETER). THE MEASURED VALUE OF V_{RESET} = = -1.98 V (-2 V TARGET PROGRAMMED WITH THE DIGITAL POTENTIOMETER). V_{READ} = 100 MV.

Fig. 3-3 summarizes the results of the characterization of 1-bit and 2-bit READ operations at different pulse widths (identical for all operations), from 1 ms down to 10 µs. For each READ operation and corresponding test condition, the distribution of V_N were recorded by repeating the programming and READ steps 10 times, thus recording 10 samples with the oscilloscope. By knowing both V_N and R_G, the current through the device is estimated as $I = V_N/R_G$. Finally, the programmed memristor resistance is calculated as $R = (V_{READ} - V_N)/I$.

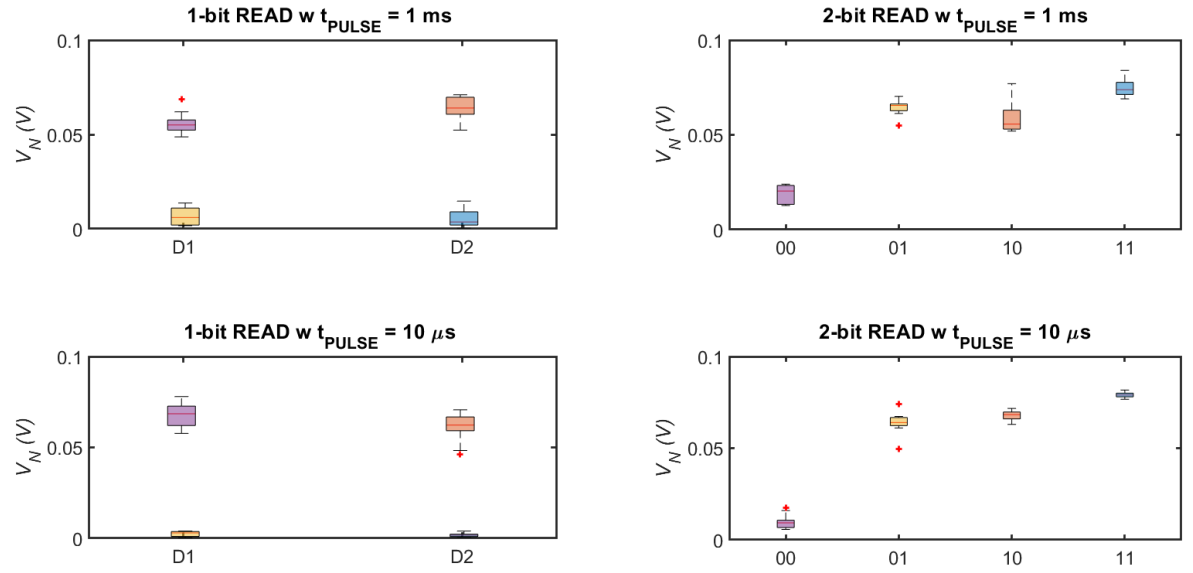

FIGURE 3-3: V_N DISTRIBUTIONS MEASURED FOR 1- (LEFT) AND 2-BIT (RIGHT) READ OPERATIONS FOR PULSE WIDTHS OF 10^{-3} S (TOP= AND 10^{-5} S (BOTTOM). FOR 1-BIT READ OPERATIONS V_N DISTRIBUTIONS AFTER SET AND RESET ARE SHOWN FOR TWO DEVICES (I.E., D1 AND D2). THE SAME DEVICES WERE THEN USED IN THE 2-BIT READ OPERATION EXPERIMENT. EACH BOX REPRESENTS 10 SAMPLES.

In the left panels of Fig. 3-3, the V_N distributions are reported with box plots, each including 10 samples, for two different devices (D1 and D2). Clearly, the top box plots are representative of the case in which the SDC

devices was in LRS while the bottom one are associated with the HRS. In all cases, and for all READ conditions, a clear distinction between the two states is obtained, which validates the feasibility of the 1-bit READ operation. Similarly, in the right panels, the V_N distributions are reported with box plots, each including 10 samples, for each possible combination of the two input bits of a 2-bit READ operation. Even in this case, it is always possible to clearly distinguish the 00 case from the others, validating the feasibility of the 2-bit READ operation as well. Finally, the data of V_N distributions in the bottom right panel of Fig. 2-2, with t_{PULSE} = 10 μs, are considered to compute the baseline Read Error Rate (RER) for the 2-bit READ operation and to estimate the optimal value of the reference voltage to be used following the procedure in [8] and in the SLIMFIT project deliverable D2.1. Specifically, the V_N distribution for the 00 case is fit with a normal distribution and the survivor function is then calculated (i.e., the complementary cumulative distribution function), see the red line in Fig. 3-4. Similarly, the V_N distribution for the 01 and 10 cases are fused together in a single distribution that is then fit with a normal distribution. The cumulative distribution function is thus estimated, see the black line in Fig. 3-4. The crossing point of the two lines in Fig. 3-4 identifies the minimum attainable RER, $RER_{MIN} = 4.7 \cdot 10^{-10}$, and the corresponding value of the reference voltage that allows obtaining the minimum RER, $V_{REF,OPT}$ = 35 mV. The analysis further confirms that reliable 2-SIMPLY operations are viable with the developed platform.

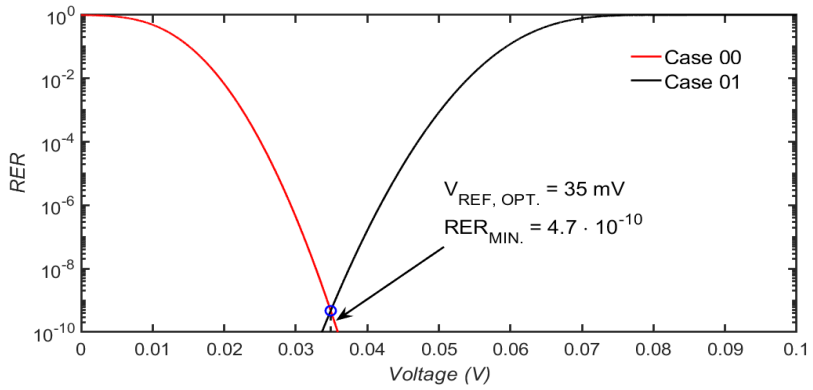

FIGURE 3-4: BASELINE READ ERROR RATE (RER) FOR THE 2-BIT READ OPERATION. THE RED LINE IS THE SURVIVOR FUNCTION OF THE NORMAL FIT OF THE V_N DISTRIBUTION OF THE CASE 00. THE BLACK LINE IS THE CUMULATIVE DISTRIBUTION FUNCTION OF THE NORMAL FIT OF THE COMBINED V_N DISTRIBUTION OF THE CASE 01 AND 10. THE CROSS-POINT OF THE TWO CURVES IDENTIFIES THE MINIMUM RER ACHIEVABLE AND THE CORRESPONDING REFERENCE VOLTAGE TO BE USED IN THE COMPARATOR. DATA OF V_N DISTRIBUTIONS WITH PULSE WIDTH = 10^{-5} S FROM FIG. 3-3 ARE CONSIDERED.

3.3 ENERGY EFFICIENCY AND PROJECTIONS

In this section, we report the measured energy for all 1-bit and 2-bit core operations. Measurements are based on the data reported in Sections 3.1 and 3.2. From the measured oscilloscope traces of each core operation, the energy per operation was estimated.

Operation	Energy (t_{PULSE} = 1 ms)	Energy (t_{PULSE} = 10 μs)
1 - bit READ (LRS)	505.6 pJ	3.93 pJ
1 - bit READ (HRS)	104.3 pJ	0.71 pJ
1 - bit SET	577.4 nJ	5.22 nJ
1 - bit RESET	68.5 nJ	991.0 pJ
2 - bit READ (Case 00)	199.6 pJ	1.40 pJ
2 - bit READ (Case 01)	610.0 pJ	5.70 pJ
2 - bit READ (Case 10)	615.5 pJ	5.12 pJ
2 - bit READ (Case 11)	693.5 pJ	6.73 pJ

TABLE 3-1: ENERGY ESTIMATES FOR ALL 1-BIT AND 2-BIT CORE OPERATIONS FOR TWO DIFFERENT PULSE WIDTH VALUES. IN ALL CASES, V_{SET} = 3 V, V_{RESET} = -2V, V_{READ} = 100 MV.

Specifically, the current was computed as $I(t) = V_N(t)/10^4\Omega$, and the energy as $E = \int_0^{t_{PULSE}} V_{TE}(t) \cdot I(t)\, dt$. Notice that the computed energy consumption takes into account also the energy dissipated on the series resistor, though excluding the overhead of the driving circuitry and of the peripheral circuitry. The energy estimates for tests with V_{SET} = 3 V, V_{RESET} = -2V, and V_{READ} = 100 mV are reported in Tab. 3-1 for two different values of the pulse width.

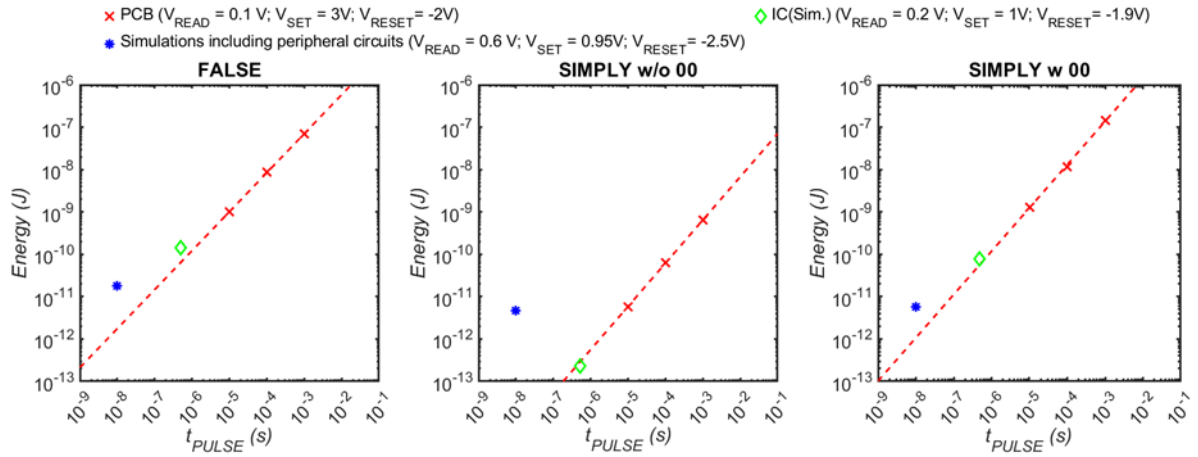

FIGURE 3-4: ENERGY PER OPERATION VS. PULSE WIDTH FOR THE FALSE OPERATION (LEFT), THE SIMPLY OPERATION WHEN EITHER INPUTS ARE NOT AT LOGIC 0 (CENTRE), AND WHEN BOTH INPUTS ARE AT LOGIC 0 (RIGHT). MEASUREMENTS OBTAINED WITH THE FPGA-BASED PLATFORM ARE REPORTED AS RED CROSSES, WHILE THE RED DASHED LINE IS A LINEAR FITTING OF THE MEASURED DATA. THE ENERGY ESTIMATES OF THE SIMULATION OF THE INTEGRATED DESIGN OF THE FULL SIMPLY CELL ARE REPORTED AS FILLED BLUE CIRCLES. THE PRELIMINARY MEASUREMENTS OBTAINED ON A TEST CHIP IN WHICH THE BUILDING BLOCKS OF THE FULL SIMPLY CELL ARE REALIZED ARE REPORTED AS GREEN DIAMONDS. THE VALUES OF V_{SET}, V_{RESET}, AND V_{READ} FOR THE DIFFERENT CASES ARE HIGHLIGHTED IN THE LEGEND.

From the data in Tab. 3-1, it is possible to estimate the energy of the FALSE operation (coincident with the 1-bit RESET) and of the SIMPLY operation. Specifically, in the case of the SIMPLY operation it is worth distinguishing between the case in which both inputs are at logic 0 and the other cases, since in the latter case the energy is coincident with the average of energy estimates for the 2-bit READ operation in the three cases reported in Tab. 3-1 as case 01, case 10, and case 11. Instead, in the former case, two terms must be computed and summed: the energy for the 2-bit READ operation in the case reported in Tab. 3-1 as case 00 and the energy for the 1-bit SET. The results are shown for three pulse widths (from 1 ms down to 10 µs) as red crosses in the panels in Fig. 3-4. The red dashed lines are linear fittings that allows extrapolating the trends down to pulse width values unattainable on the developed FPGA-based platform but typical of the IC realization, confirming the dominant role of the pulse width on the energy consumption. This is further corroborated by the comparison with the results of the simulations of the integrated design of the full SIMPLY cell (for a pulse width of 10 ns) reported in [8] and in D2.1, also shown in the panels in Fig. 3-4 as filled blue circles. It is worth noting that the energy consumption of the full SIMPLY cell for the FALSE operation is only slightly larger than the projections obtained with the linear fitting of the experimental data measured with the developed FPGA-based platform. This is due to differences of the two memristive technologies employed. Specifically, the Knowm memristors exhibit higher resistance values in both LRS and HRS than the one employed in the integrated design of the full SIMPLY cell, which is naturally associated with lower power consumption. In addition, the series resistor features a higher resistance than that exhibited by the tail transistor in the integrated design, which further contributes to the energy discrepancy. Finally, the energy overhead of the driving circuitry (i.e., the tri-state buffers) is included in the energy estimates of the integrated design but not in the measurements performed with the FPGA-based platform. Similar results are obtained when evaluating the energy consumption of the SIMPLY operation when both inputs are at logic 0. Indeed, in this case the energy consumption is dominated by the 1-bit SET contribution, for which the same considerations as above apply. Interestingly, when evaluating the energy consumption of the SIMPLY operation when either input is not at logic 0, the discrepancy between the projections obtained with the linear fitting of the experimental data measured with the developed FPGA-based platform and the energy estimated of the integrated design of the full SIMPLY cell is quite larger. Indeed, in this case the energy overhead of the driving circuitry, of the reference voltage generator, and of the comparator (included only in the estimates of the integrated design of the full SIMPLY cell) is non-negligible, and together with the differences in *i*) the overall resistance of the memristor/resistor (or tail transistor) series, and *ii*) the different read voltage values, determines a wide discrepancy

between the energy estimates. Nicely, all projections are well aligned with preliminary measurements obtained at the device level (i.e., without the overhead of the peripheral circuitry) performed on a test chip in which the building blocks of the integrated design were realized (green diamonds in Fig. 3-4), confirming that the energy scaling of the SIMPLY solution is feasible.

Finally, the KPIs identified in the proposal, besides the logic retention discussed in Section 2.2, included the energy efficiency in terms of throughput per unit power, the target value of which was set to 1 TOPS/W at a power consumption of 20 μW. From Tab. 3-1 and Fig. 3-4 it can be appreciated how the energy per operation scales approximately linearly with the employed pulse width, which implies a relatively constant power dissipation associated to each operation. For the estimation of this KPI, we assume the S-FALSE and the 2-SIMPLY operations as equally likely to occur at runtime. We also consider that the logic input bit combinations of either operation are equally likely to occur. It is thus possible to estimate, from the data in Tab. 3-1, the average power consumption expected under an arbitrary workload which is found to be ≈ 90 μW and essentially invariant with the pulse width. By assuming a runtime frequency of 50 MHz (corresponding to a 10 ns pulse width at 50% duty cycle), the projected throughput per unit power at a power consumption of 90 μW is ≈ 0.56 TOPS/W, which is already close to the target value identified in the proposal. The projected value at 20 μW power consumption is ≈ 2.5 TOPS/W, which indeed exceeds the target in the proposal. It has to be specified that this figure of merit, by design and in-line with what specified in the proposal, does not take into account the energy overhead of the peripheral circuitry. Nevertheless, as shown in Fig. 3-4 and discussed earlier in this deliverable, the overhead is significant only for operations in which neither SET not RESET steps are performed, i.e., the 2-SIMPLY operation when either input is at logic 1. Conversely, the overhead is small for the more energy-hungry operations that entail SET or RESET steps, which constitute the energy efficiency bottleneck. Thus, it is expected that the energy overhead of the peripheral circuitry will have a relatively mild impact on the overall energy efficiency metric at least in the frequency range explored in this project.

4 CONCLUSIONS AND FUTURE DEVELOPMENTS

In this deliverable we discussed the general structure of the developed evaluation platform able to control an array of memristors to realize the core operations of the SIMPLY logic scheme, together with the results of the device characterization and of the verification of the feasibility of the SIMPLY core operations. The platform was designed, realized and tested, and then used to successfully verify the correct execution of the SIMPLY core operations. For all of the 1-bit and 2-bit core operations, the energy consumption was measured and then compared with the results from the simulations of the integrated design of the full SIMPLY cell and with preliminary measurements from a test chip on which the building blocks of the full SIMPLY cell were realized. The energy scaling trends with the pulse width confirms the energy efficiency advantage of the SIMPLY architecture compared to traditional digital systems. Nevertheless, it is possible to envision interesting additions and future developments, which constitute the ground for activities beyond the horizon of the SLIMFIT project with the aim of capitalizing on the obtained results. Specifically, to further enhance the testing of SIMPLY operations on packaged devices, several improvements to the PCB can be envisaged. First, a minor but beneficial upgrade would be the addition of a dedicated reference-voltage circuit for the digital potentiometers. This would simplify and make more consistent the generation of the SET, READ, and RESET voltages, which currently depend on the externally supplied 3.3 V source. A more substantial improvement concerns the grounded pull-down resistor which could be replaced with an NMOS transistor. This modification would enable the implementation and direct verification of read-margin optimization strategies such as boosted sensing and dynamic transistor biasing. As with the other voltage values controlled through the FPGA, the gate-bias voltage of the transistor could be conveniently set using a digital potentiometer followed by a buffer. Additional improvements can be achieved by refining the control signals for the multiplexers (MUXs) and buffers, and by making slight adjustments to the PCB connections. At present, the “0” input of each MUX is left floating to produce a high-impedance (Hi-Z) state. However, during the testing phase it was noticed that Hi-Z could be more robustly enforced by properly driving the enable pins, which are currently tied to the state of the FPGA board’s control switches through the FPGA firmware. This would allow the “0” input of the MUX to be tied to ground, while the MUX selectors are driven to ensure that the TE node returns to 0 V immediately after a programming pulse, thereby reducing capacitive delay effects. Furthermore, the grounded terminal of the pull-down resistor (or equivalently, the source of the NMOS transistor) could be actively driven using an appropriate circuit. This modification would facilitate the testing of circuit configurations that operate from a single power-supply rail. Finally, the PCB layout could be optimized to ensure reliable operation at higher switching speeds, which are however limited by the employed FPGA model, which in turn could be updated to a faster unit.

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